



## Functional Description

The process starts with the first message block of sixteen words being clocked into the core. The INIT signal is asserted at the start of each message. The MD5 core is ready to accept data when REQ is asserted.

Each 32-bit word is clocked into the core on the rising edge of CLK when ACK is asserted. After a block of 16 words has been input, REQ is deasserted as the MD5 core computes the message digest. After another 49 clock cycles, the message digest for that 16 word block is computed and REQ is asserted again to indicate that more words can be clocked in.

The standard specifies that the maximum number of bits in the message is  $2^{64} - 1$ . Therefore the maximum number of 32-bit words that can be clocked in is  $2^{59} - 1$ . The core can cope with any number of words up to  $2^{59} - 1$  being input.

The LAST signal is asserted when clocking in the last word. At least one pad, and two length words need to be added to the end of the message as part of the MD5 calculation.

Note that the BYTE signal is considered valid and sampled by the core when the LAST signal is high. This signal is used by the core to determine how many bytes in the last word are part of the input data.

If the total number of input words plus three is not a multiple of 16, the core adds additional pad bytes to calculate the message digest as specified in the standard.

The two Length words that contain the bit-length of the original message are also added by the core.

The 160-bit message digest is output on A, B, C, D when READY is asserted.

## Export Permits

The core is available for export to all countries for non-military applications, except to the following countries:

Cuba	Iran	Iraq	Libya
North Korea	Sudan	Syria	

It is the customer's responsibility to check with relevant authorities regarding the re-export of equipment containing the MD5 technology.

## Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

The core has been verified through extensive synthesis, place and route and simulation runs. It has also been embedded in several products, and is proven in FPGA technologies.

## Deliverables

The core is available in ASIC (RTL) or FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source
- Sophisticated HDL Testbench (self checking)
- C Model & test vector generator
- Simulation script, vectors & expected results
- Synthesis script
- User documentation