IPB-G726

G.726 ADPCM Voice Codec

Overview

The G.726 ADPCM Voice Codec (IPB-G726) is a speech codec designed to work as an audio offload engine in a multi-processor environment, in both FPGAs and ASICs.

The coder commands, settings and state can be written/read by means of a status and control register file. After the Start command, the core simultaneously encodes 4 PCM channels (linear or logarithmic) and decodes 4 ADPCM channels, using the (AD)PCM Data I/O interface. The coder can be halted by the Stop command. The algorithm runs on the Fireworks low complexity CPU for flexibility. For high channel counts the SideWorks reconfigurable accelerator is also used. Transfers between CPU, I/O and accelerator are handled by a specific DMA engine.

The feature set of the IPB-G726 emphasizes complete support of the ITU G.726 specification. Low frequency, small silicon area and small memory footprint have been targeted to lower the system cost and power consumption. Low latency and low memory bandwidth have also played an important role in defining the feature set.

Features

- Real time voice coding of 4 duplex channels @10 MHz
- Complete support of the ITU G.726 specification
- Supports linear and logarithmic PCM
- Number of channels can be customized upon request
- Supports burst or continuous data flows
- Configurable compression rate
- µ Law and A Law support for inputs and outputs
- Configuration, Control and Status register file for core operation
- Parallel audio interfaces easy to integrate

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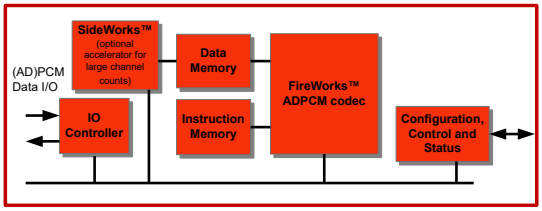
Benefits

- Compact hardware implementation – fits economically in FPGAs and ASICs
- Low operation frequency
- Extremely low power consumption
- Small external memory footprint

Block Diagram



FPGA Implementation Results

FPGA	Slices / LEs	BRAM	DSPs	Fmax (MHz)
Spartan-6™	1300	8x16Kb	4	80
Virtex-5™	1080	4x36Kb	4	100
Virtex-6™	1050	4x36Kb	4	120
Cyclone III™	2400	16xM9Ks	4	80

ASIC Implementation Results

Technology node	Area (mm^2)	mclk Fmax (MHz)
TSMC 130 nm	0.11	224
TSMC 90 nm	0.08	365
TSMC 65 nm	0.04	558

Deliverables

- RTL or FPGA netlist
- Vivado or Quartus project
- Documentation
- Driver
- Testbench
- Simulation models and test cases

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