Moortec
Global In-chip Monitoring

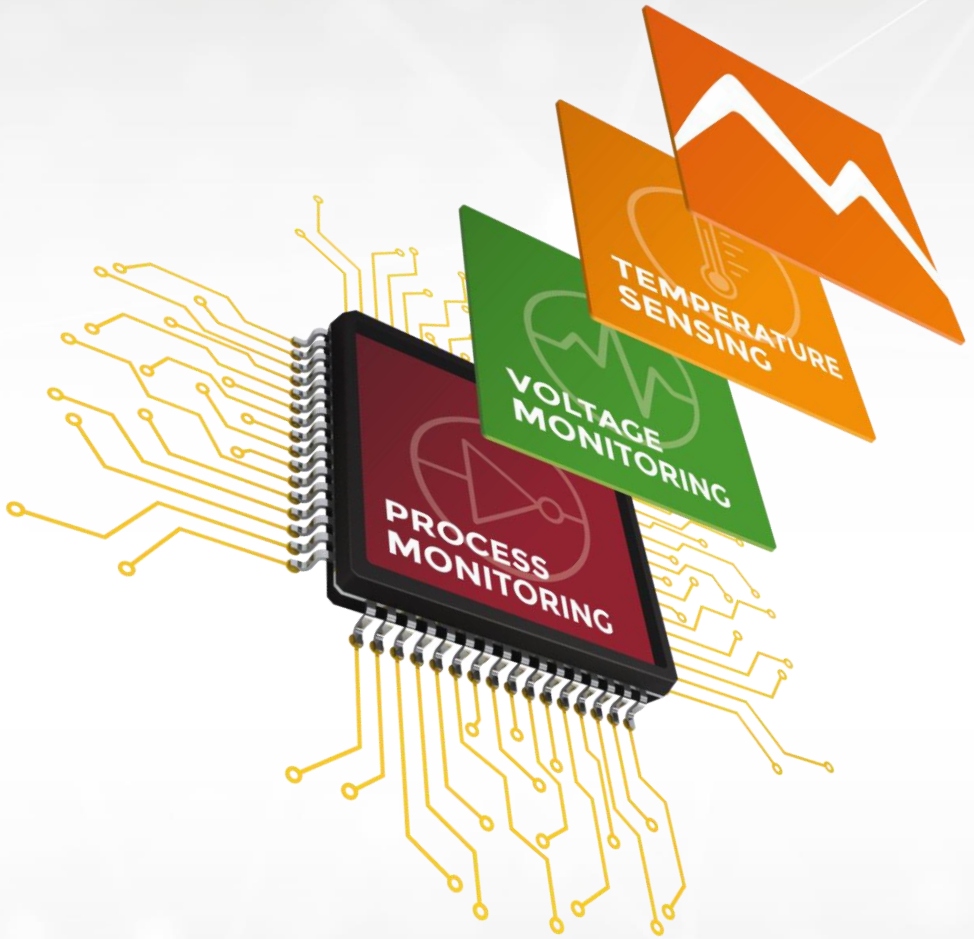
In-Chip Monitoring Subsystem Solutions

SPINNAKER SYSTEMS

Moortec Semiconductor

Founded in 2005, headquarters in UK.

- In-Chip Monitoring Subsystem Solutions
- SoC Optimisation and Enhanced Reliability
- Design support and guidance
- Trusted IP Vendor with global customer base
- The only PVT dedicated IP vendor



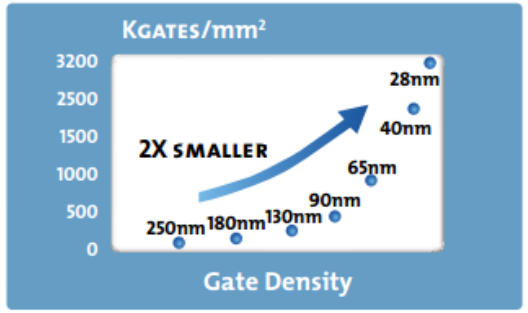
Challenges

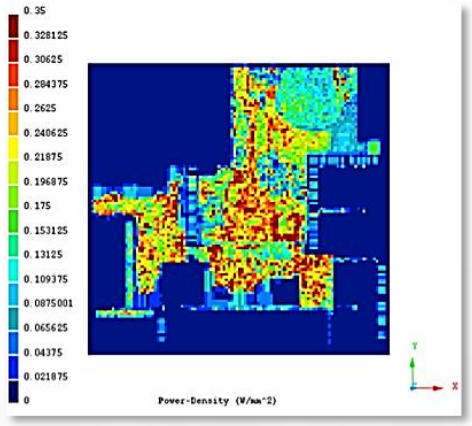
Scaling effect 65nm, 40nm, 28nm,16nm, 7nm

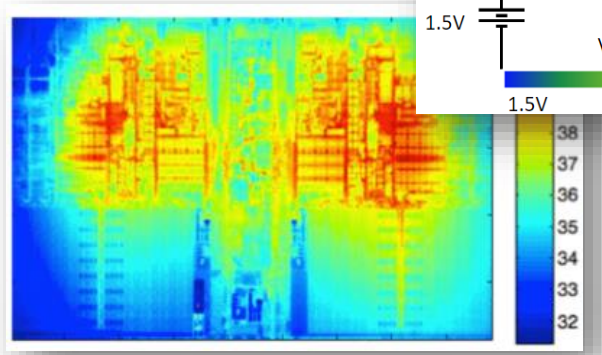
Gate Density

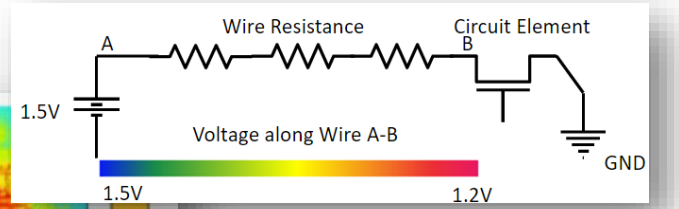
Power Density
Complexity
Process Variance

Thermal Density
IR Drop & Noise
Timing Closure









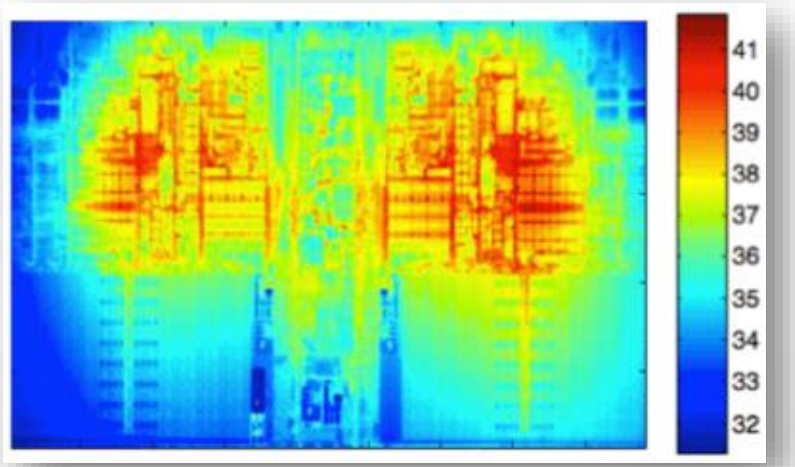
FAST

TYP

SLOW

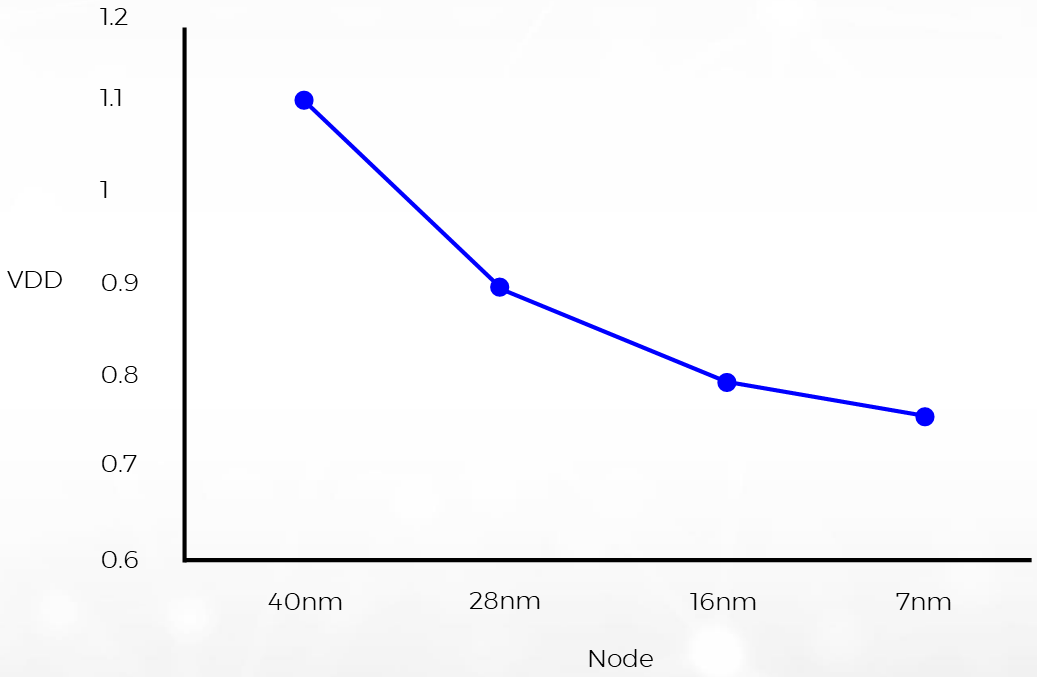
Thermal Challenges

- FinFET structures less able to dissipate heat
- Density leading to increased thermal challenges
  - Electrical OverStress (EOS)
  - Electromigration (EM)
  - Hot carrier aging
  - Increased Negative Bias Temperature Instability (NBTI)
- Device leakage causes heat and heat causes more leakage (Thermal runaway)
- Leakage to increase when we move from one FinFET node to the next



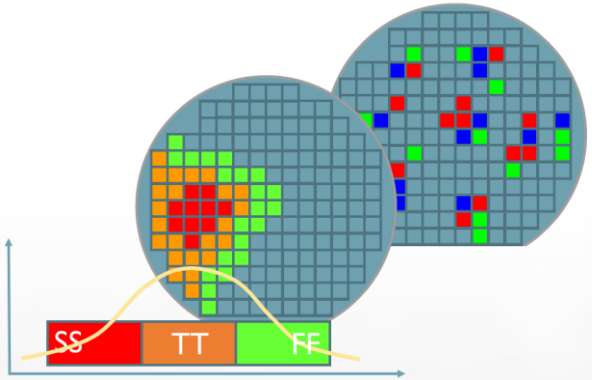
Supply Challenges

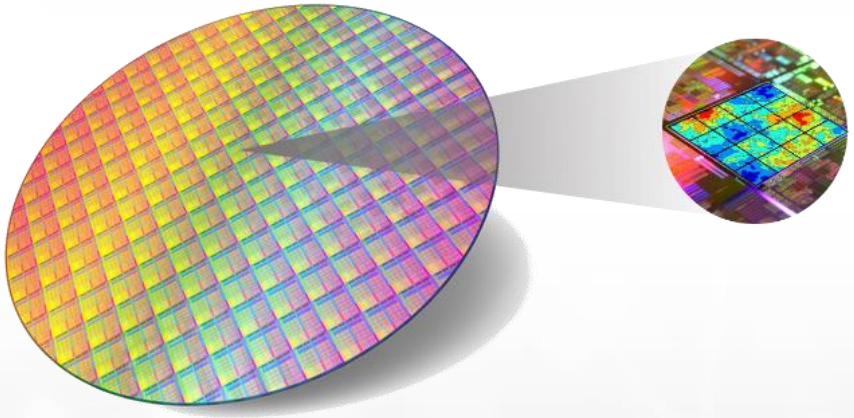
- Reduction in supplies
- Interconnect resistance
- Increased gate capacitance
- Dynamic versus static power
- Dynamic IR drop
- Electromigration (Higher current densities)



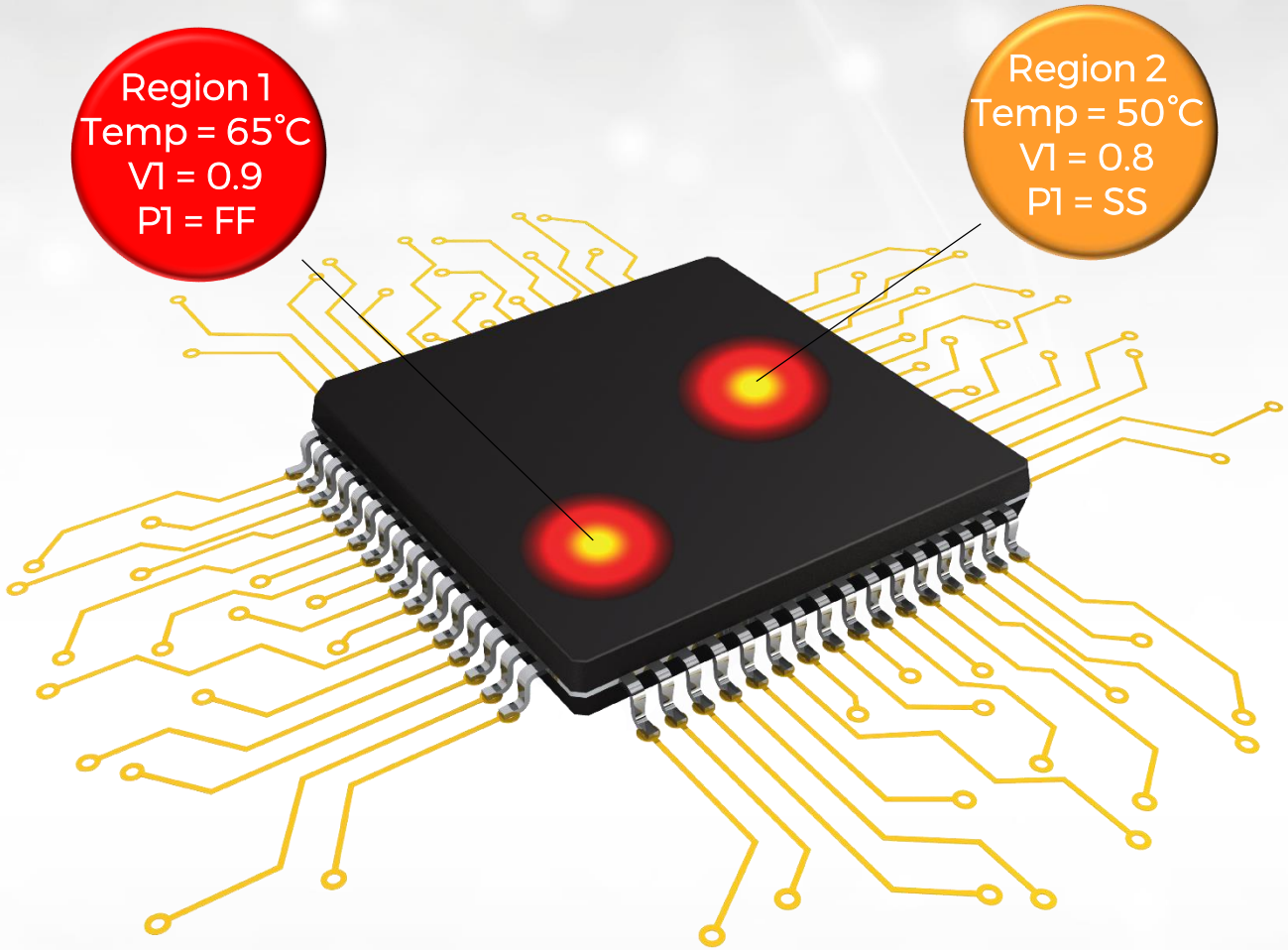
Process Challenges

- New process variations mechanisms
- Middle of line & multiple patterning
- Multiple Vts in single voltage domain
- Ageing





Process Challenges - Timing Closure



Key Challenge for Advanced Nodes

- Timing closure
- Low yield (through timing violations)

Region 1

T1 = 65C
V1 = 0.9V
P1 = FF

Region 2

T2 = 50C
V2 = 0.8V
P2 = SS

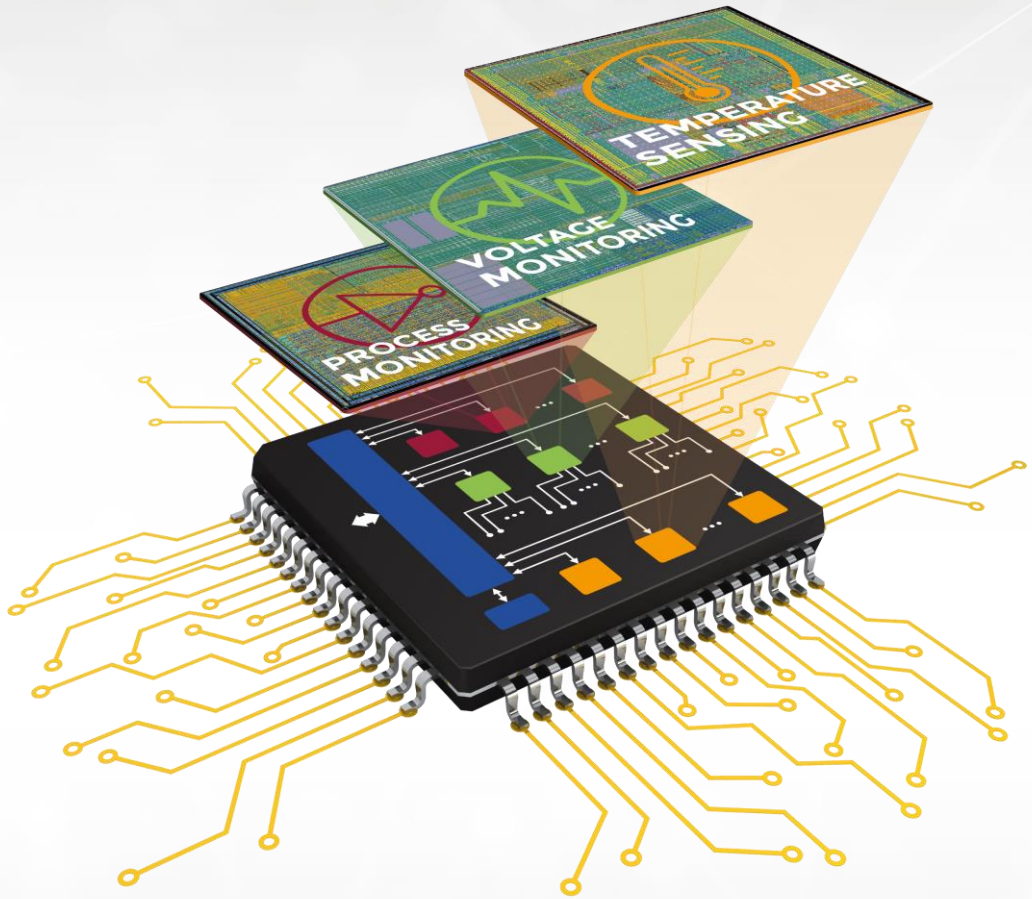
Requirement from IC Design Community

Enhanced Chip Lifetime
- Thermal & Voltage Stress
- EM Management

Individual Chip Optimisation
- Dynamic and Adaptive Schemes
- DVFS & AVS

Failure Prediction & In-Field Monitoring

Applications:
- Datacentre & Enterprise
- Mobile Communications
- Telecommunications
- Consumer (DTV)
- Automotive

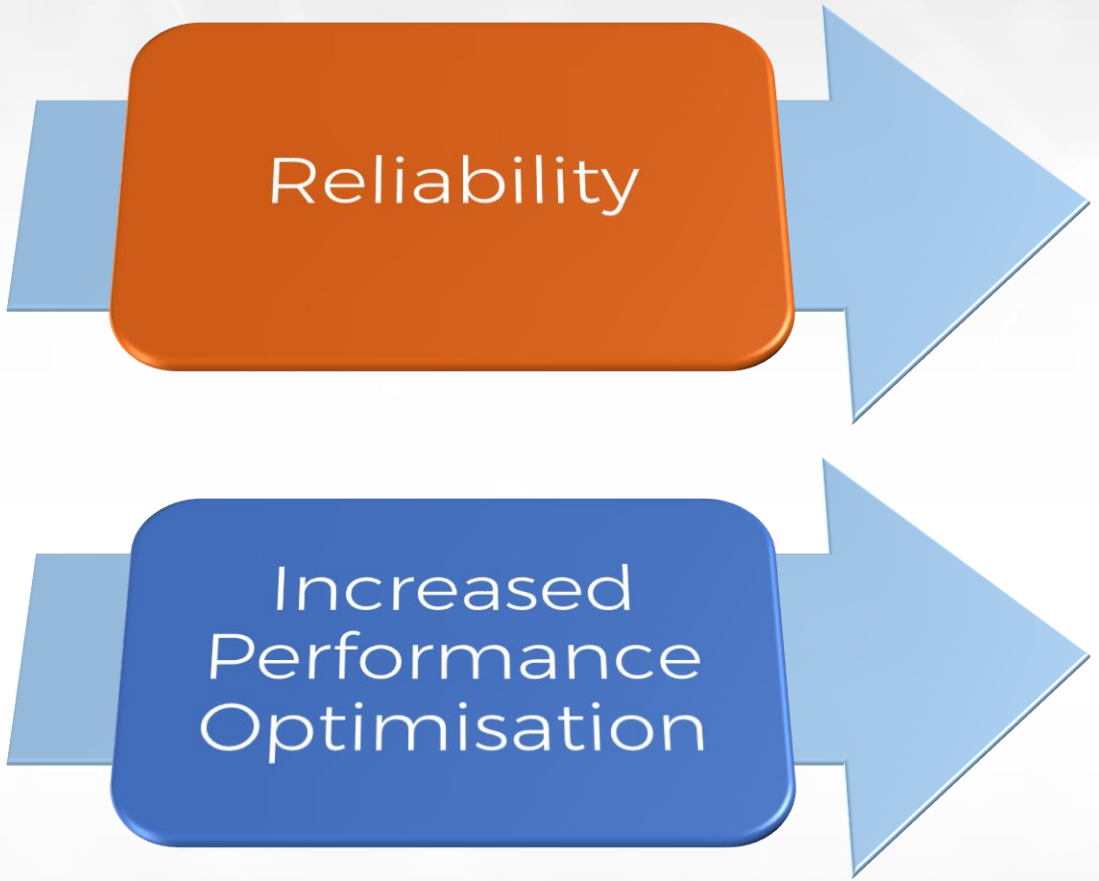


The Moortec Solution

High Accuracy

Highly Featured

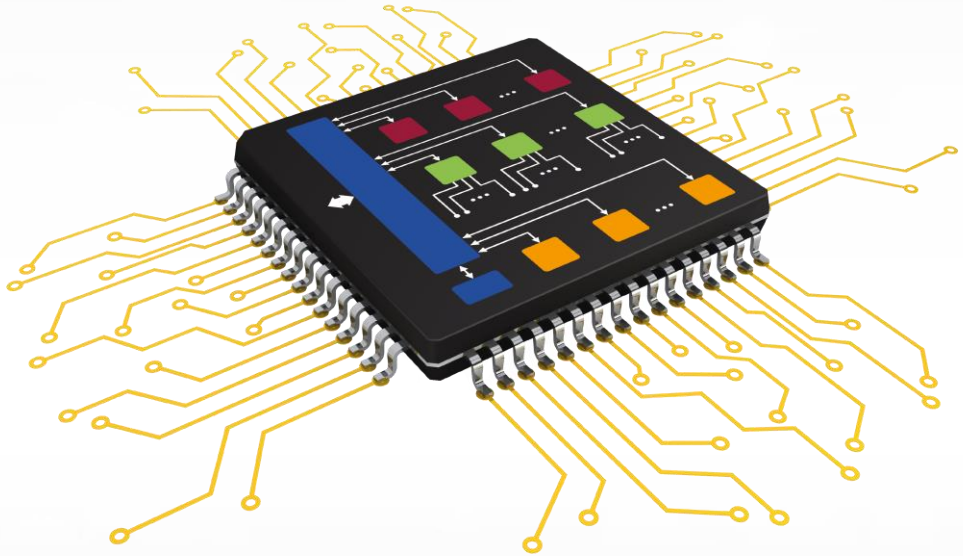
Well Supported



Life Time Monitoring
Manage Conditions
Physical Protection

Per Chip Optimisation
Power
Data Throughput
Better Case Design

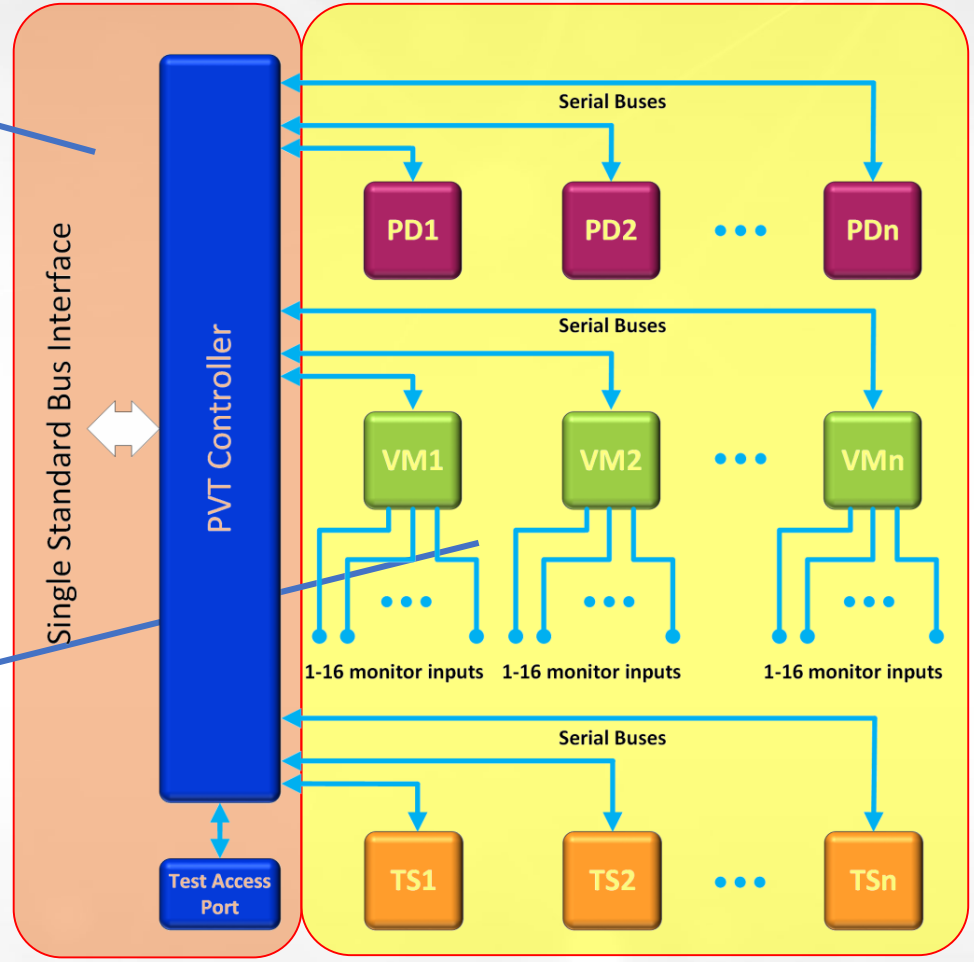
In-Chip Monitoring Subsystem Solution



Soft Delivery:
User Guide
RTL / Constraints

Hard Macro Delivery:
Datasheets
Integration Guidelines
Verilog / Timing Files
GDSII / LVS&DRC Reports

Interface Options:
AMBA APB
USoC
SPI
IMGBUS



USP Analysis

Technical

- Accuracy
- Standard CMOS
- Easy Calibration (single point)
- Testability (SCAN & Test modes)
- Self-checking / Monitor health status

Support

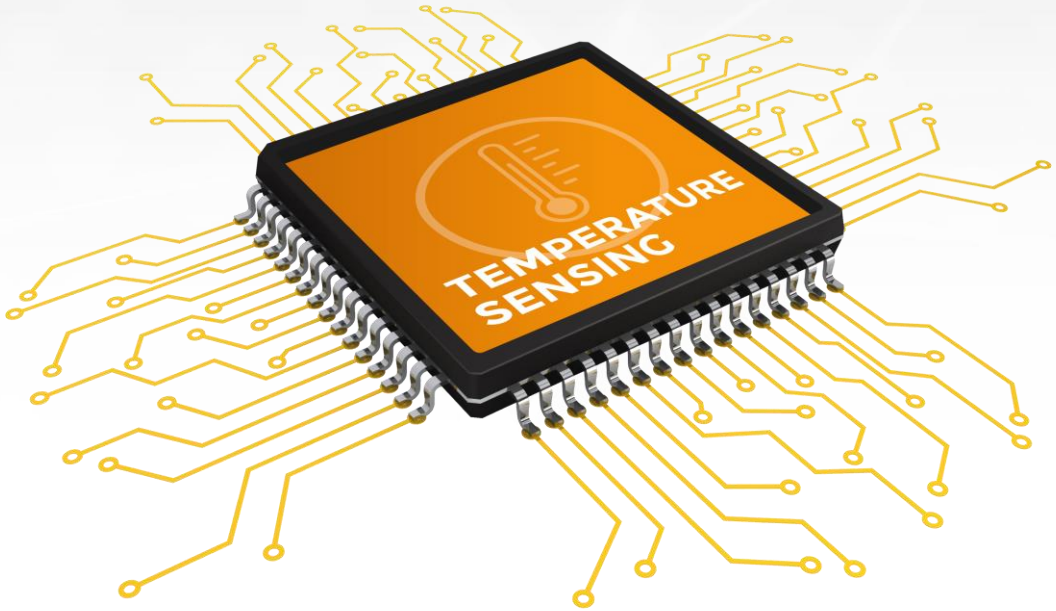
- Experience
- Design & integration guidance
- Expertise on macro placement
- Production results analysis
- Excellent Support

Temperature Sensors

Moortec's temperature sensor product family:

Series (High Accuracy, 28nm, FinFET)

- Accuracy +/-3C, +/-1C calibrated
- vcal Calibration scheme
- Single temperature point
- 'Don't care' calibration temperature
- Resolution of 0.06C
- Size 240um x 200um
- Analogue test bus (characterisation & debug)
- APB, I2C optional interface
- Enhanced testability (including SCAN)
- Accompanying PVT controller (APB, IEEE1500)
- Self-checking (fault flag)
- 12-bit / 10-bit / 8-bit modes (for faster sampling)

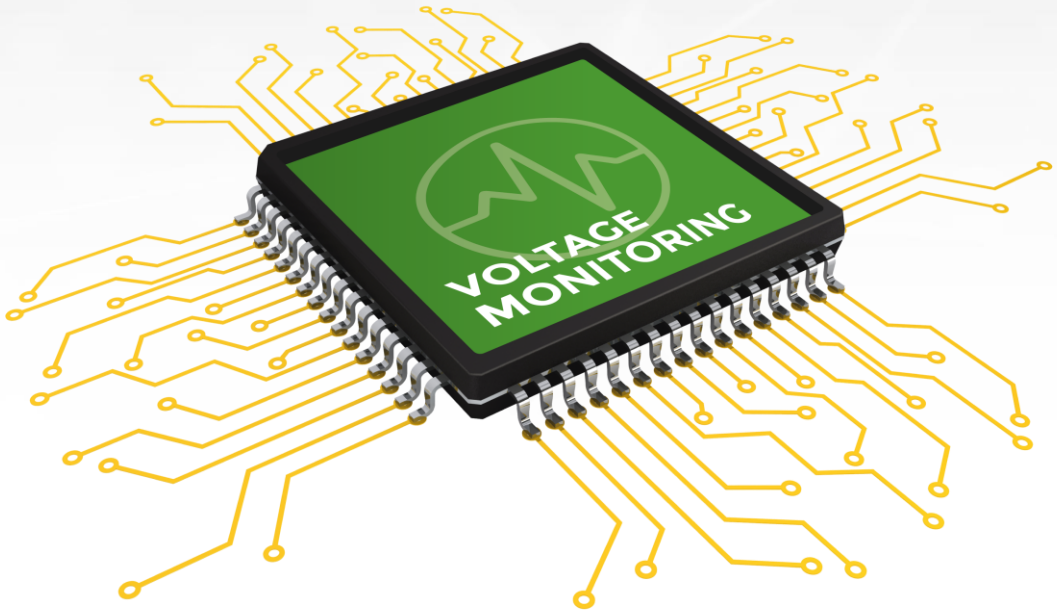


Voltage (Supply) Monitors

Monitoring
- IR Drop
- Core and IO supply domains
- AVS

Detection
- Supply ‘events’
- Perturbations
- Transients and supply spikes (roadmap)
- +/-1% or +/-0.6% accuracy
- +/-1mV accuracy for IR drop analysis

Multi-Domain Monitoring
- Up to 9 channels (28nm, series 1)
- Up to 16 channels (FinFET, series 2)



Process Monitors

Description:

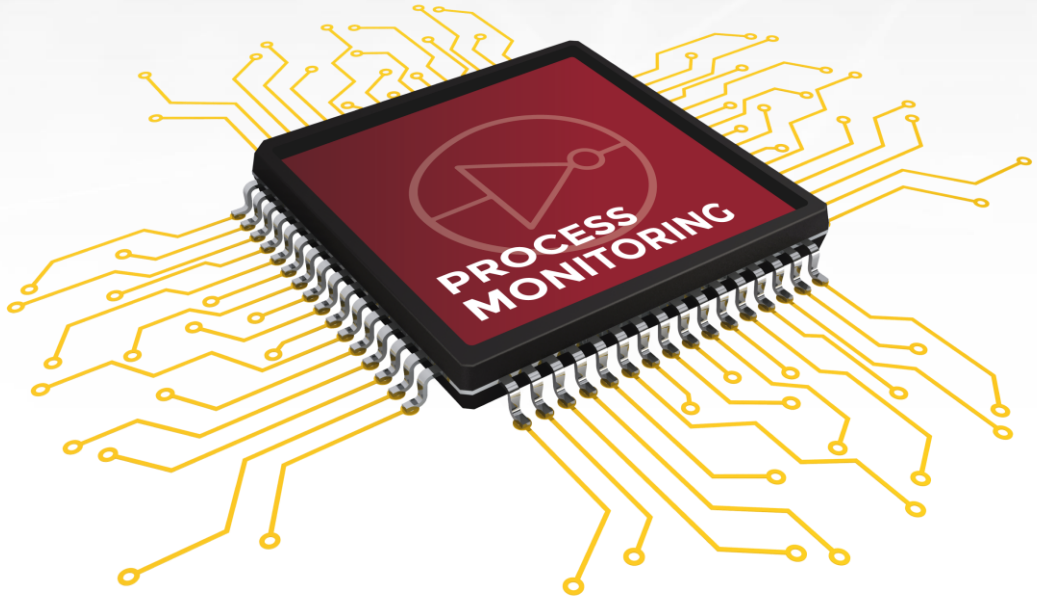
- Multiple internal delay chains (ring oscillators)

Configurations:

- Multiple internal delay chains (ring oscillators)
- Transistor: LVT, SVT, HVT, uLVT, iLVT, Thick-Ox
- Fan-out / Loading (4 at each stage)
- Interconnect delay (metallisation)

Applications:

- Speed binning (characterisation)
- Age monitoring
- Critical voltage & timing analysis
- AVS



PVT Controller with Standard Interfacing

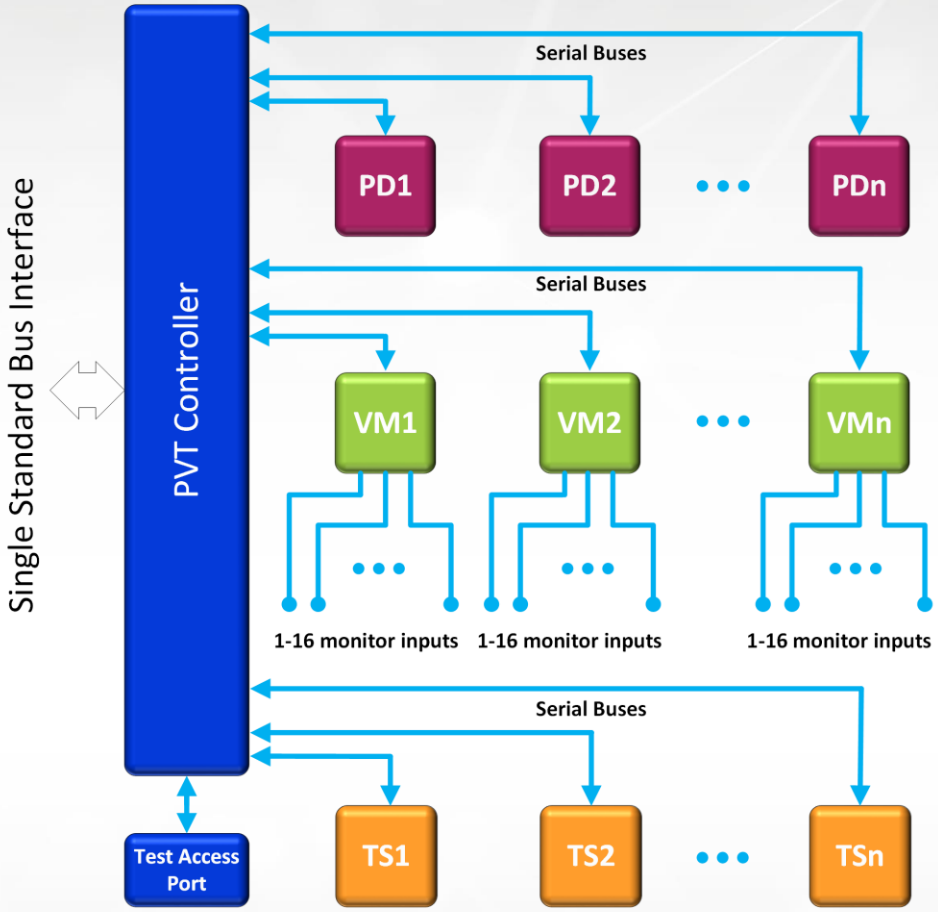
Single Interface, Multiple PVT Instances

Key Features

- Monitoring of up to:
  - 24 x Process Monitors
  - 8 x Voltage (Supply, VDD) Monitors
  - 8 x Temperature Sensors (High Precision)
- Temperature & Voltage Alarms / Hard Stops
- PVT Statistics (max min sample values, sample counters)
- Clock synth
- Auto-polling
- Soft and hard lock of register access
- iJTAG access support

Applications

- DVFS+
- Clock Speed Optimisation
- Power Optimisation
- Silicon Characterization
- Increased Reliability & Device Lifetime



Summary - Choosing Moortec

Best available PVT Monitoring IP

- High Accuracy
- Highly Featured
- Well Supported

Partnerships

- Foundry alliances
- Partner Collaborations
- University partnerships

TSMC Open Innovation Platform® Partner of the Year New IP Award - 2016

SPINNAKER SYSTEMS

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PRiME
www.prime-project.org