Verific®
Design Automation

HDL Source Code Components

- VHDL IEEE 1076-1993 parser, analyzer, and elaborator
- Verilog IEEE 1364-1995/2001 pre-processor, parser, analyzer, and elaborator
- Automatic FSM/RAM extraction from RTL
- EDIF 2.0 reader
- SDF reader
- Liberty reader
- Hierarchical, technology independent database

"Quartus II, Altera's flagship design software includes integrated VHDL and Verilog HDL technology from Verific. To date, we have shipped this to approximately 17,000 customers. Verific's software meets the high standard of quality our customers have come to expect from us."

Misha Burich, Senior VP
Software Engineering,
Altera

"We have worked with Verific's VHDL parser from the early days of Verix, our formal RTL verification system. The software is reliable, well engineered, and made the task at hand a lot simpler. Our time to market savings were substantial."

Rajiv Kumar, COO and
co-founder, Real Intent

Verific Design Automation develops, markets, and supports HDL Component Software which enables its customers to develop advanced *HDL based products* quickly and at low cost.

Designed to be platform-independent, *Verific's* HDL Component Software is distributed as *C++ source code* and compiles on Solaris, HP-UX, Linux, and Windows platforms.

Verific's HDL Component Software is in production and development use today at a number of companies worldwide, from EDA start-ups to established Fortune 500 semiconductor vendors. Applications vary from formal verification (model as well as equivalence checking) to synthesis, emulation, in-circuit debug, and design-for-test.

Benefits of HDL Component Software

Time to Market

- At least 6 to 9 month head start with production proven RTL technology
- No need to recruit and staff your own HDL software team
- No need for extensive test and debug of your HDL solution

Focus

- Concentrate on the strategic, differentiated core of your application
- Don't waste time and talent on non-strategic HDL software

Quality

- Prevent lost sales due to immature HDL front-end
- Prevent high support costs due to bugfix releases and workarounds

License Models

- All license are Source Code, allowing you full control over modifications, extensions, integration, and compilation.
- Various license models available:
  - + Time-based licenses with no upfront cost, cancel any time
  - + Perpetual, royalty free licenses
  - + Royalty bearing licenses
- We will find a license model that fits your needs.

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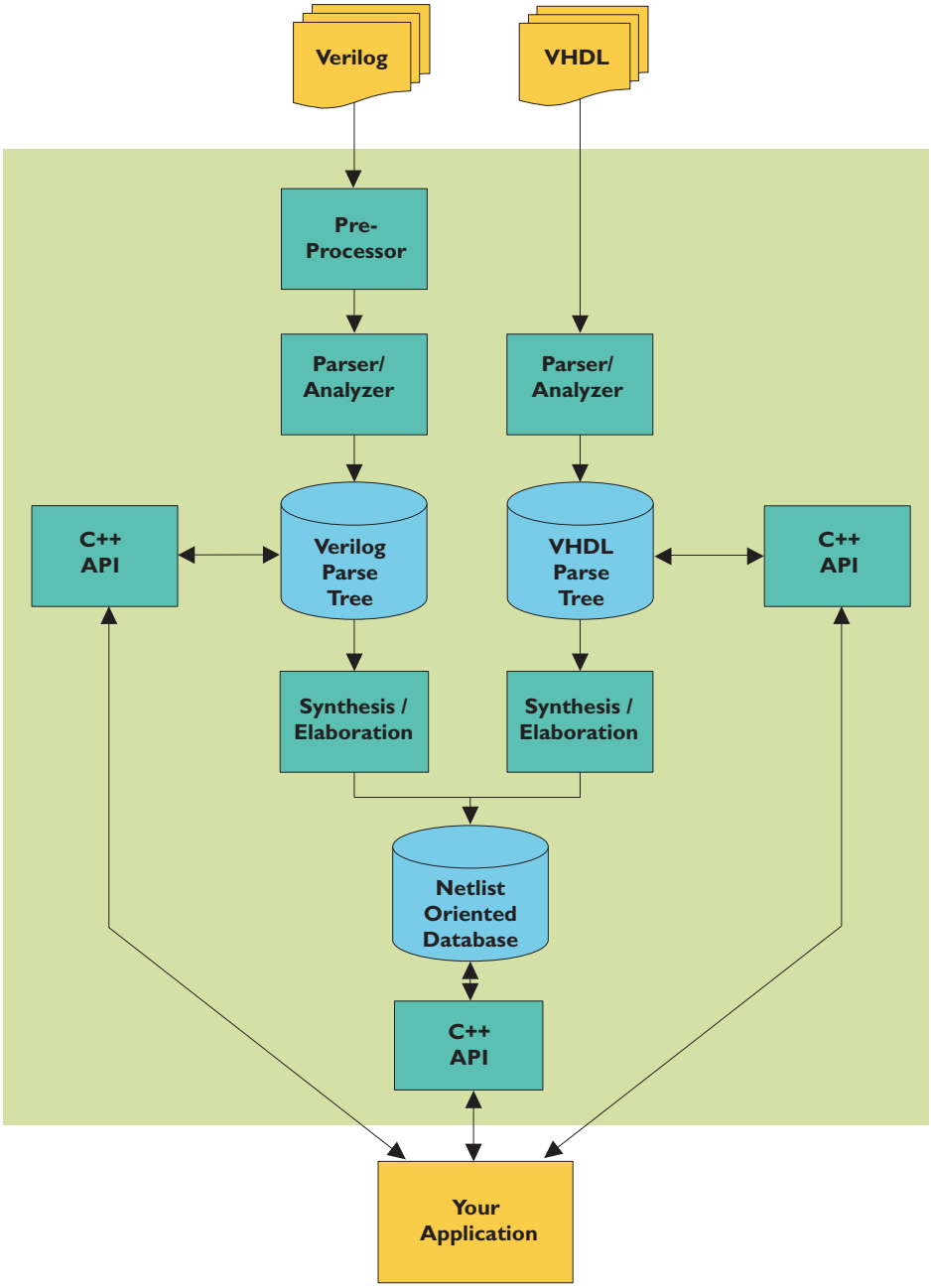

"As a performance leader in Hardware Acceleration, Tharas was pushed by its customers to add VHDL support. After extensive evaluations, we chose Verific as our VHDL front-end. Verific has provided outstanding support, and has proved to be a great R&D partner."

Ramesh Narayanaswamy,
VP engineering,
Tharas Systems

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Verific's software is integrated in a variety of EDA products, including:

Altera	Quartus II
@HDL	@Verifier
Philips ED&T	RTL DfT
Real Intent	Verix
Tharas Systems	Hammer
Translogic	Ease

Applications include FPGA synthesis, Model Checking, Functional Verification, Hardware Acceleration, RTL Debug, Logic Equivalence Checking, RTL Floorplanning, HDL Entry, Design for Test, and Asynchronous Circuit Analysis

"We, as well as our end-users, are very impressed with the language support, overall quality, and speed of the software."

Mario Konijnenburg,
Philips ED&T

"We chose to purchase software from Verific Design Automation for reasons of product quality and time to market. We found the software well architected and very reliable, and as a result we easily saved 12 months of engineering development time."

Willem Gruter, Vice-President Engineering,
Translogic

"Verific's source code saved us at least 6 months of development time right from the start of our EDA project."

Oriol Roig, Manager Software Development,
Theseus Logic

Strategic Versus Commodity Technology

"Technology that does not differentiate your product from your competitors should be classified as context and outsourced with all possible speed, thereby freeing up time, talent, and management attention to the next wave of core differentiation."

Geoffrey A. Moore,
Living on the Fault Line

Production Proven HDL Front-Ends

More than 10 companies are shipping products incorporating Verific's Verilog HDL and VHDL front-ends, with a combined customer base of more than 20,000 users. The principal developer of Verific's HDL Software Components wrote VHDL and Verilog HDL parsers, analyzers, and elaborators for two different synthesis products at a major EDA company prior to architecting the Verific solution. Instead of writing your own, you can buy and incorporate the C++ source code, fully tested and production proven, from the experts in HDL language synthesis. And, because Verific ships Source Code, you still retain full control over all modifications, extensions and integration.

Royalty-free, Time-based and Perpetual Source Code Licenses

Verific Design Automation ships its software as C++ source code, including makefiles for Unix and Windows platforms. Most of our customers choose our royalty-free time-based licenses or our royalty-free perpetual licenses. Maintenance and support contracts are also available.

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Verific Design Automation, Alameda, CA (510) 522-1555 www.verific.com

VHDL Reader

- Parses, analyses and elaborates 10,000 lines/second RTL, 30,000 lines/second flat-netlist code. (Average throughput, 2 Ghz Xeon, Red Hat Linux 8.0.)
- 100% VHDL 93 (IEEE 1076-93) as well as VHDL 87 (IEEE 1076) language coverage.
- Includes synthesis subset checking.
- Wide language subset support for elaboration, including IEEE 1164, multiple libraries, records, multi-dimensional arrays, generics, configurations, user-defined and overloaded functions/procedures/types, variable-indexing etc.
- Support for all standard and de-facto standard synthesis packages.
- Support for all Cadence, Mentor Graphics, and Synopsys synthesis pragmas.
- Downstream error handling support with line/file origination storage in RTL database.
- Application specific compile and run-time switches (don't care info, object preservation, etc.)

Verilog Reader

- Parses, analyses and elaborates 15,000 lines/second RTL, 30,000 lines/second flat-netlist code. (Average throughput, 2 Ghz Xeon, Red Hat Linux 8.0).
- 100% Verilog IEEE 1364-1995 / 2001 language coverage.
- Includes synthesis subset checking.
- Built-in Verilog pre-processor.
- Wide language subset support for elaboration, including memory, named ports, tasks, functions, variable-indexing, string constants, UDP tables, etc.
- Verilog XL compliance with unknown module instantiation, and -y/-v file search mechanisms.
- Support for all Cadence, Mentor Graphics, and Synopsys synthesis pragmas.
- Downstream error handling support with line/file origination storage in RTL database.
- Application specific compile and run-time switches (don't care info, object preservation, etc.)

RTL Database

- Average memory usage approximately 300 bytes / gate.
- Full hierarchy support, with grouping/ungrouping, etc.
- Full support for any number of libraries, and no restrictions on library interaction (instantiations across different libraries).
- Support for buses.
- Compact storage of line and file origination info from RTL Readers.
- Simple and clean data model and Procedural Interface for easy integration with your existing database.

Support and Maintenance

- On-line, customer accessible defect and enhancement tracking.
- Standard monthly releases with enhancements and improvements
- 24 hour turnaround for critical defects

About Verific Design Automation

Verific Design Automation was founded in 1998 by EDA industry veteran Rob Dekker. Prior to founding Verific, Dekker was a Software Developer, Manager, and Director at Exemplar Logic where he was the architect and a primary developer of Leonardo, Exemplar's flagship synthesis product which has sold over 10,000 copies to date.

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June 2003